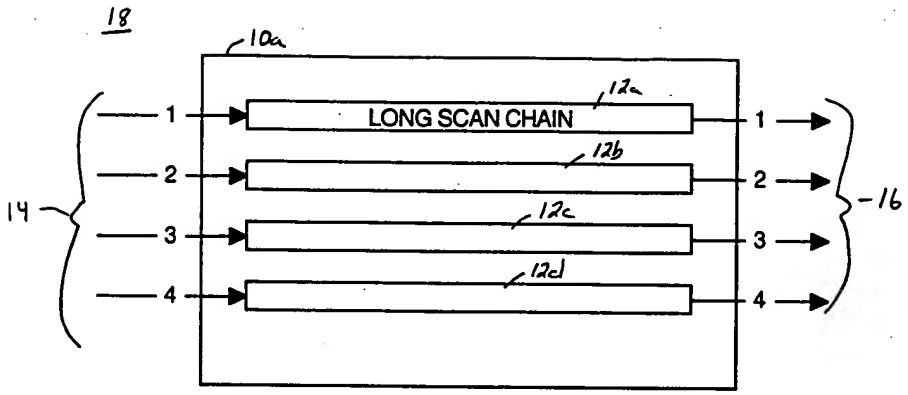
18
10a
12a
LONG SCAN CHAIN
12b
12c
12d
1
2
3
4
14
16

FIG 1A

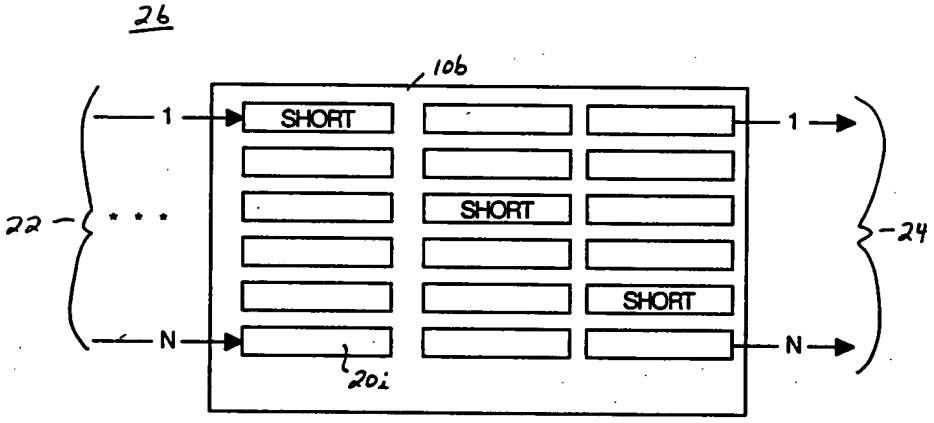
26
10b
SHORT
SHORT
SHORT
1
N
22
24
20i

FIG 1B

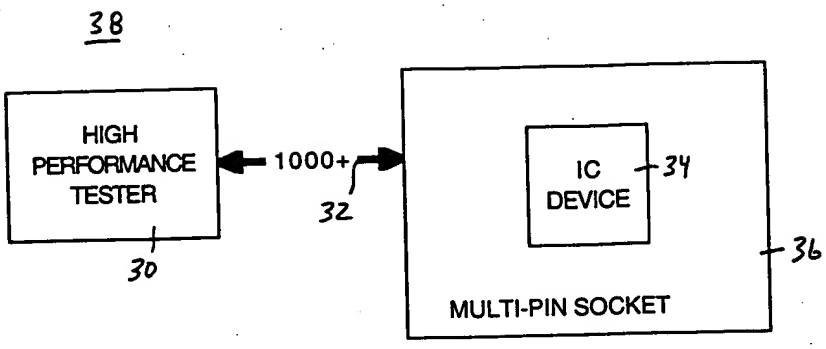
38
HIGH PERFORMANCE TESTER
1000+
32
30
IC DEVICE
34
36
MULTI-PIN SOCKET

FIG. 1C

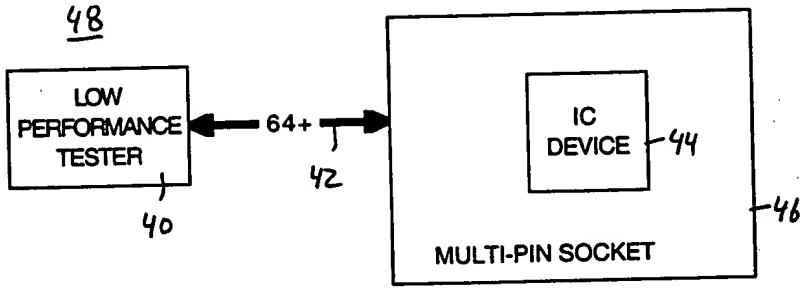
48
LOW PERFORMANCE TESTER
64+
42
40
IC DEVICE
44
46
MULTI-PIN SOCKET

FIG. 1D

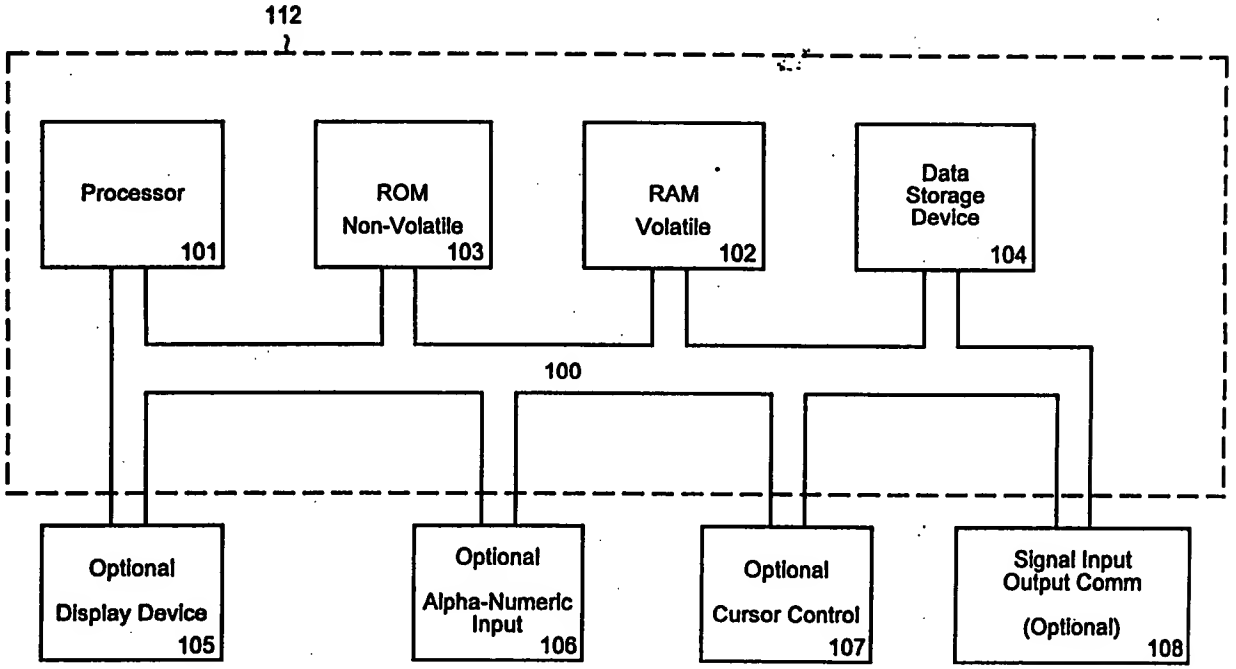
112
Processor
101
ROM
Non-Volatile
103
RAM
Volatile
102
Data
Storage
Device
104
100
Optional
Display Device
105
Optional
Alpha-Numeric
Input
106
Optional
Cursor Control
107
Signal Input
Output Comm
(Optional)
108

FIG. 2

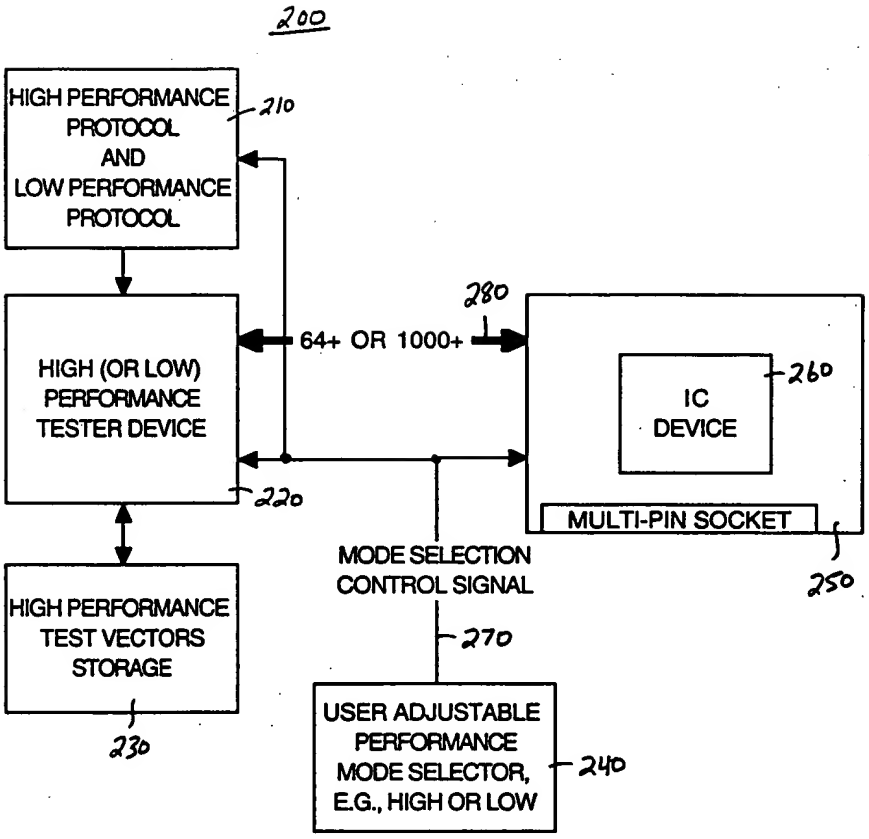
200
HIGH PERFORMANCE PROTOCOL AND LOW PERFORMANCE PROTOCOL
210
HIGH (OR LOW) PERFORMANCE TESTER DEVICE
220
64+ OR 1000+
280
IC DEVICE
260
MULTI-PIN SOCKET
250
MODE SELECTION CONTROL SIGNAL
270
HIGH PERFORMANCE TEST VECTORS STORAGE
230
USER ADJUSTABLE PERFORMANCE MODE SELECTOR, E.G., HIGH OR LOW
240

FIG. 3

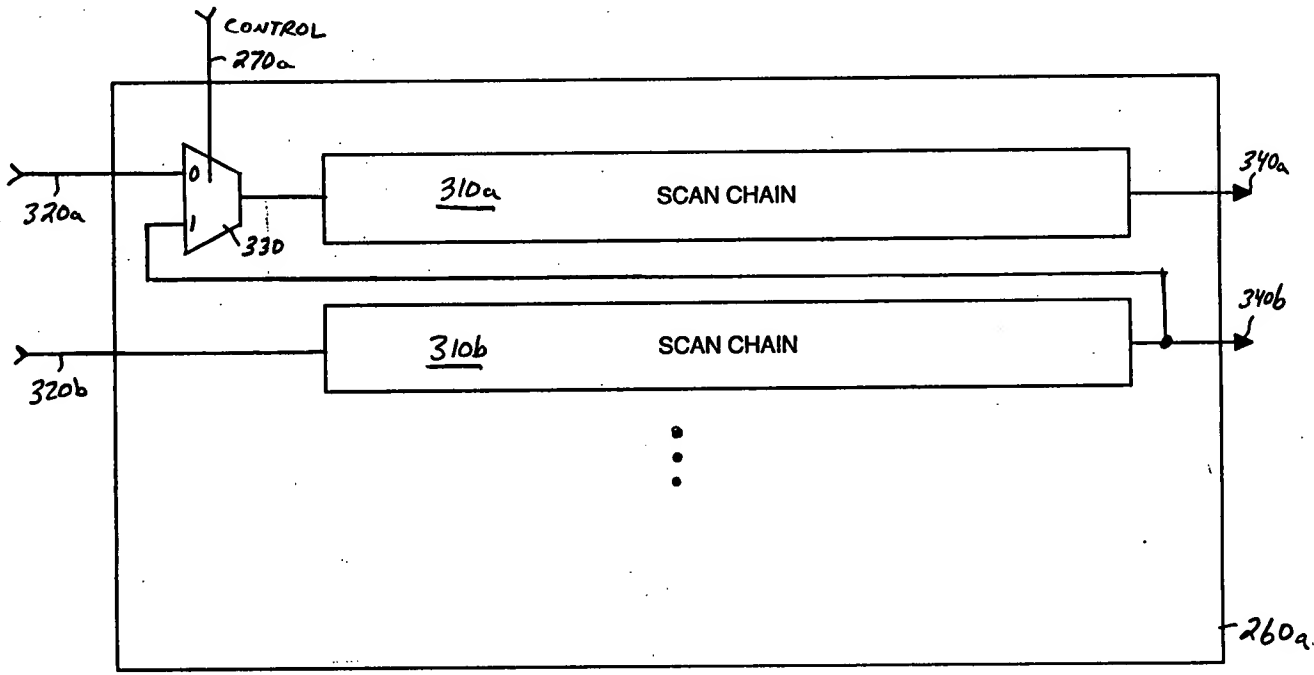

FIG. 4A

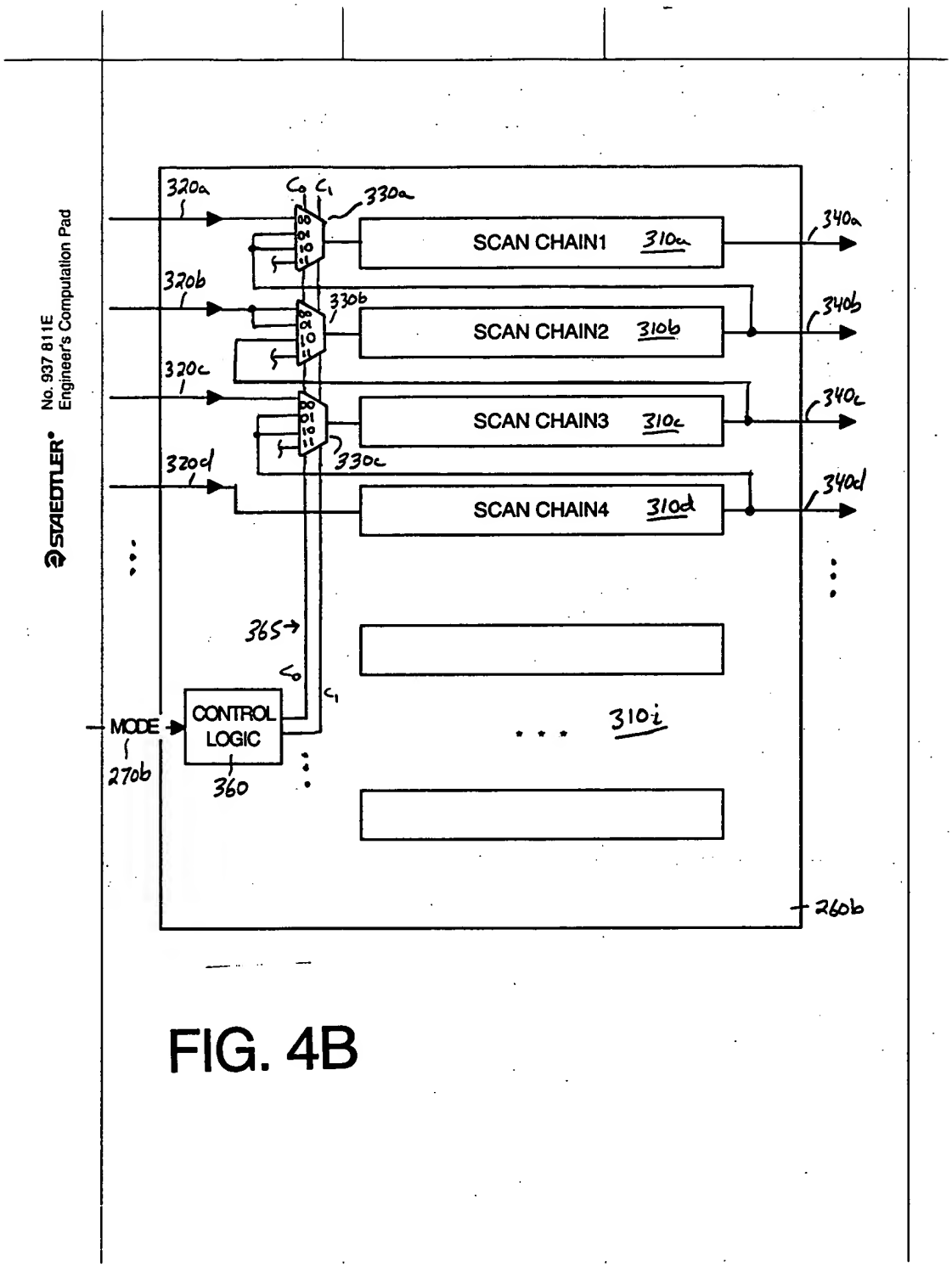
320a
C_0
C_1
330a
SCAN CHAIN1 310a
340a
320b
330b
SCAN CHAIN2 310b
340b
320c
SCAN CHAIN3 310c
340c
330c
320d
SCAN CHAIN4 310d
340d
365
C_0
C_1
MODE
270b
CONTROL LOGIC
360
310i
260b

FIG. 4B

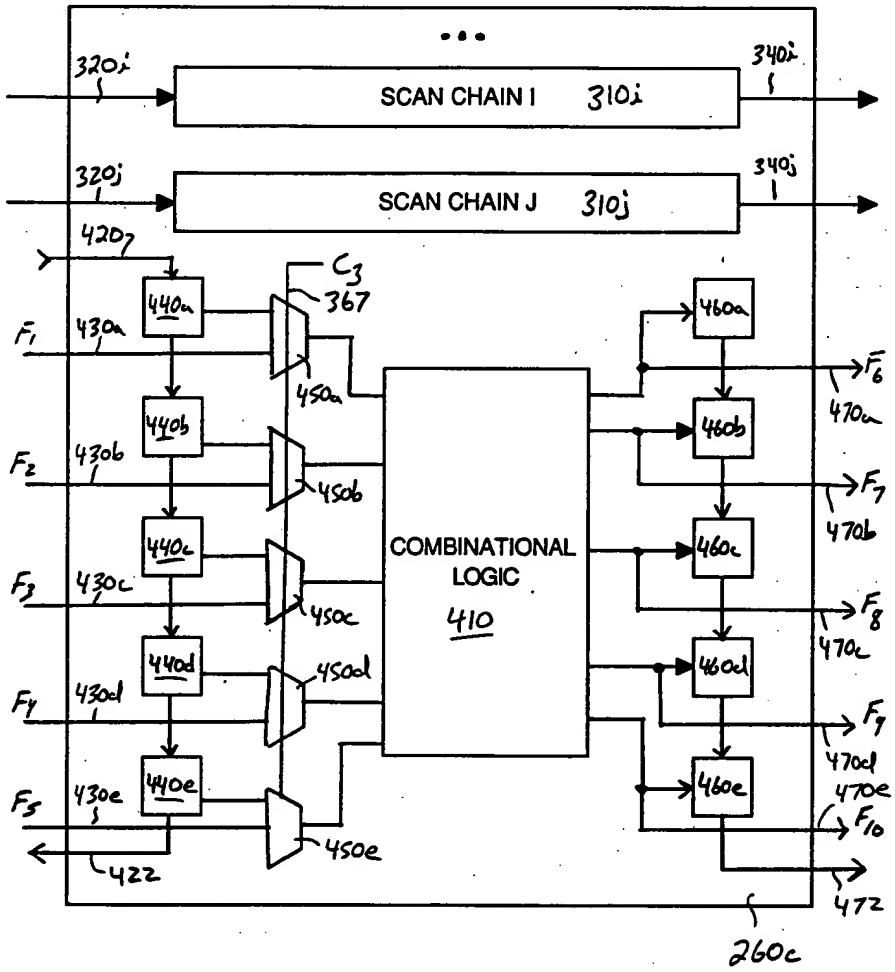

FIG. 5

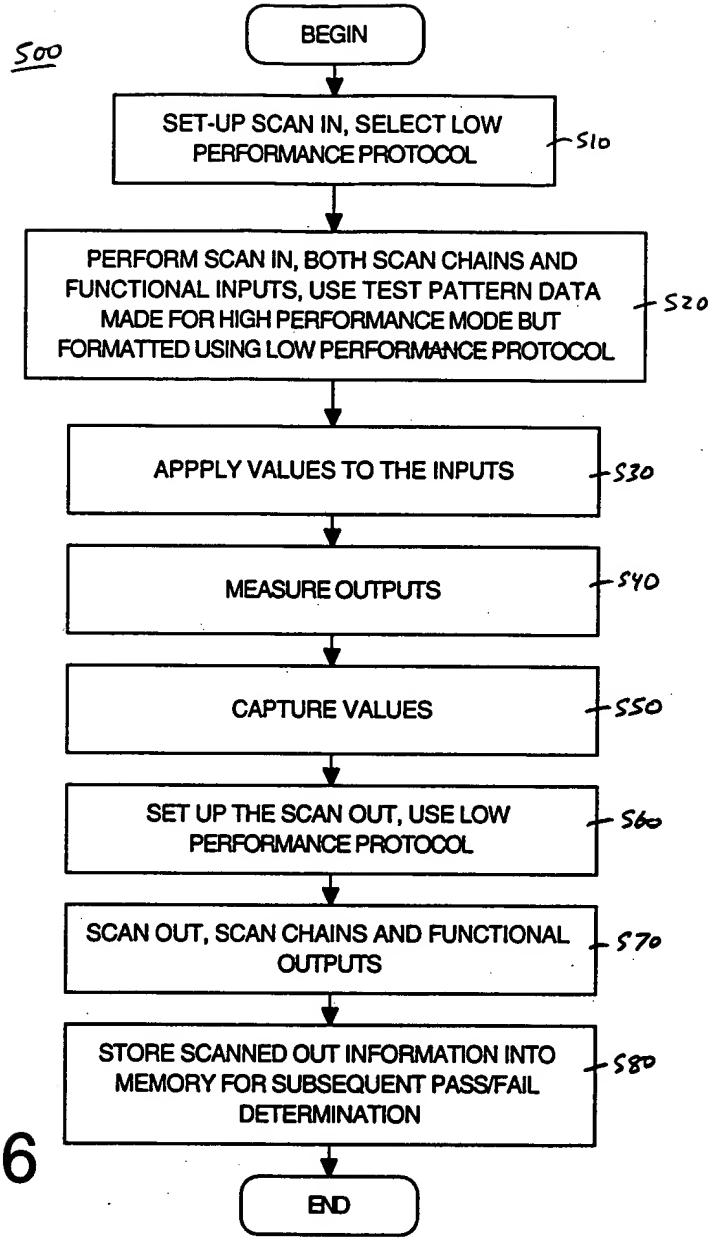
500
BEGIN
SET-UP SCAN IN, SELECT LOW PERFORMANCE PROTOCOL
510
PERFORM SCAN IN, BOTH SCAN CHAINS AND FUNCTIONAL INPUTS, USE TEST PATTERN DATA MADE FOR HIGH PERFORMANCE MODE BUT FORMATTED USING LOW PERFORMANCE PROTOCOL
520
APPPLY VALUES TO THE INPUTS
530
MEASURE OUTPUTS
540
CAPTURE VALUES
550
SET UP THE SCAN OUT, USE LOW PERFORMANCE PROTOCOL
560
SCAN OUT, SCAN CHAINS AND FUNCTIONAL OUTPUTS
570
STORE SCANNED OUT INFORMATION INTO MEMORY FOR SUBSEQUENT PASS/FAIL DETERMINATION
580
END

FIG. 6

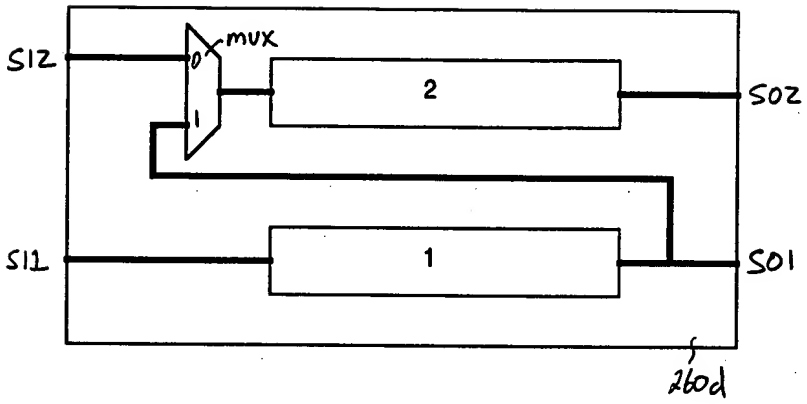

FIG. 7A

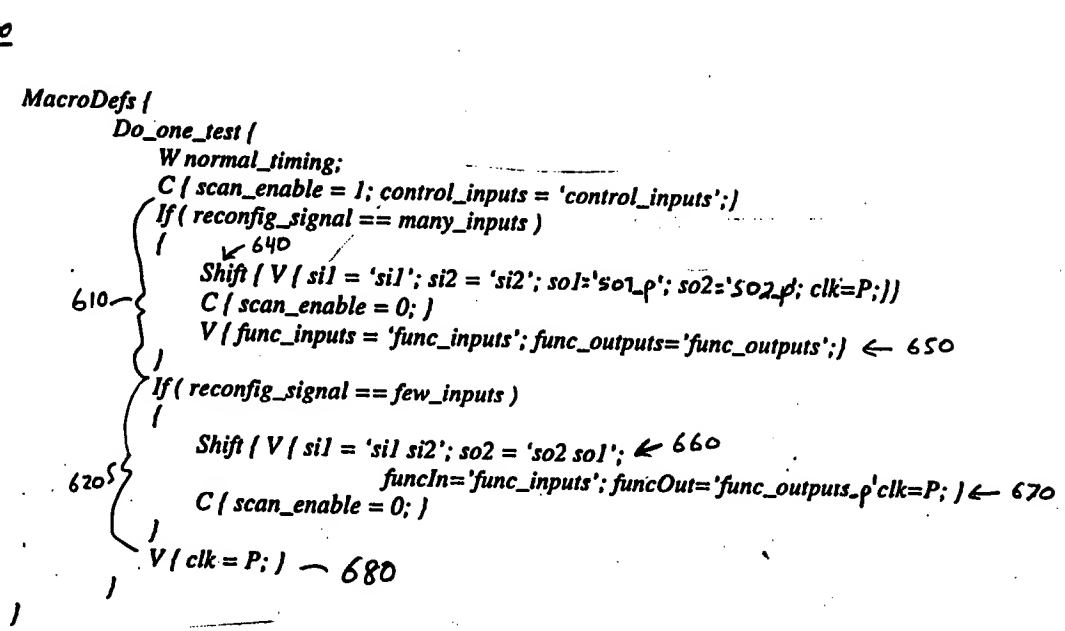

FIG. 7B